## AMENDMENTS TO THE CLAIMS

1. (currently amended) An integrated circuit, configured to process microphone signals, where the integrated circuit comprises:

a preamplifier with an amplifier section which has a differential input comprising a first input (+) and a second input (-) and an output ($\varphi$; $\varphi$*), and with a feedback filter network coupled between the output ($\varphi$; $\varphi$*) and the second input (-); where the first input (+) to the amplifier section is coupled to an input ($\phi$) of the preamplifier for receiving a microphone signal ~~has an input impedance which by means of the input impedance of the amplifier section is substantially isolated from the feedback network with respect to input impedance~~; and where the preamplifier has a frequency-gain transfer function which suppress low frequencies in a stop band relative to higher frequencies in a pass band; and where the preamplifier is configured to provide a common-mode differential output signal in the stop band and a differential-mode differential output signal in the pass band; and

an analogue-to-digital converter coupled to receive ~~an~~ the differential output ~~anti-aliasing filtered input~~ signal, as an anti-aliasing filtered signal, from the preamplifier and to ~~providing~~ provide a digital output signal.

2. (original) An integrated circuit according to claim 1, where the preamplifier is configured to provide a differential output signal ($\varphi$, $\varphi$*) by a first and a second amplifier section,

where the preamplifier has a differential mode transfer function which comprises a band-pass characteristic ($A_{DM}$), and

where the preamplifier comprises a feedback filter network which establishes filter feedback paths (a-b; c-d) which couple outputs to respective inverting inputs of the amplifier sections, and which establishes a filter interconnection path (a-c), which interconnects the inverting inputs.

3. (currently amended) An integrated circuit according to claim 1 ~~or 2~~, where a lower cut-off frequency ($F_{P1}$) of the filter realized by the preamplifier is located below the lower corner frequency of an audio band.

4. (currently amended) An integrated circuit according to ~~any of~~ claims ~~1 to 3~~, where the preamplifier has a differential mode transfer function ($A_{DM}$) which comprises a band-pass characteristic with an upper cut-off frequency ($F_{P3}$; $F_{P2}$) located below half the sampling frequency ($F_S$) of the analogue-to-digital converter.

5. (currently amended) An integrated circuit according to ~~any of~~ claims 1 ~~to 4~~, where the preamplifier has a differential mode transfer function ($A_{DM}$) which comprises a band-pass characteristic, which has a nominal pass-band ($F_{P1}$ - $F_{P2}$) and a gain plateau band ($F_{Z2}$ - $F_{P3}$), where the nominal pass-band extends over audio band frequencies and where the gain plateau band extends over frequencies above the audio band up to an upper cut-off frequency ($F_{P3}$).

6. (currently amended) An integrated circuit according to ~~any of~~ claims ~~1 to 5~~, where the preamplifier has a common-mode transfer function ($A_{CM}$) which comprises a low-pass characteristic.

7. (currently amended) An integrated circuit according to ~~any of~~ claims ~~1 to 6~~, where the preamplifier has a common-mode transfer function ($A_{CM}$) which comprises a stop-band characteristic ($F_{Z1'}$ - ; $F_{Z1'} - F_{Z2'}$), and where a flat gain response is provided for low frequencies ($DC - F_{P1'}$).

8. (currently amended) An integrated circuit according to ~~any of~~ claims ~~1 to 7~~, where the preamplifier has a common-mode transfer function ($A_{CM}$) and a differential mode transfer function ($A_{DM}$) which are configured such that its common-mode gain ($A_{CM}$) prevails at low frequencies ($DC$-$F_{P1'}$) whereas its differential mode gain ($A_{DM}$) prevails at audio band frequencies ($F_{AL}$-$F_{AU}$).

9. (currently amended) An integrated circuit according to ~~any of~~ claims 1 ~~to 8~~, where additionally the common-mode gain ($A_{CM}$) prevails at frequencies above an upper cut-off frequency ($F_{P2}$, $F_{P3}$) of the band-pass characteristic.

10. (currently amended) An integrated circuit according to ~~any of~~ claims 1 ~~to 9~~, where a phase-shifter is cross-coupled between the output of a first amplifier section and an input of a second amplifier section.

11. (currently amended) An integrated circuit according to ~~any of~~ claims 1 ~~to 10~~, where a phase-shifter is coupled between respective inputs (-) of the respective amplifier sections.

12. (currently amended) An integrated circuit according to ~~any of~~ claims ~~1,~~ ~~to 11~~ where the preamplifier comprises a DC off-set circuit integrated with the feedback filter (Z1; Z1,Z1*,Z2) to provide a DC shift at the output of the preamplifier.

13. (currently amended) An integrated circuit according to ~~any of~~ claims ~~1,~~ ~~to 12~~ comprising a DC off-set circuit integrated with the feedback filter and configured to provide a differential mode DC shift at the output of the preamplifier.

14. (currently amended) An integrated circuit according to ~~any of~~ claims ~~1,~~ ~~to 13~~, where the analogue-to-digital converter comprises a sigma-delta modulator.

15. (original) An integrated circuit according to claim 14, where the sigma-delta modulator comprises a switch-capacitor sampler, which samples the differential signal ($\varphi$, $\varphi$*) provided by the preamplifier to provide a single ended input signal for the sigma-delta A/D conversion, and samples a DC voltage level ($V_{Ref\Sigma\Delta}$) such that the single ended input signal is superimposed on the sampled DC voltage level.

16. (original) An integrated circuit according to claim 15, where the sampler comprises a summing amplifier which is an integrated portion of the sampler and the sigma-delta modulator loop.

17. (original) An integrated circuit according to claim 16, where the summing amplifier is provided with an integration error feedback signal of the sigma-delta modulator via a first series capacitor and where the DC voltage level is provided to the summing amplifier via a second series capacitor.

18. (currently amended) An integrated circuit according to ~~any of~~ claims 1 ~~to 17~~, where the analogue-to-digital converter comprises a sigma-delta modulator, and where a DC off-set voltage level input to the sigma-delta modulator is chosen such that a low-frequent pulse input to and processed by the preamplifier provides idle-mode tones above the audio band.

19. (original) A microphone comprising an integrated circuit as set forth in any of the above claims and a condenser microphone element configured to provide a microphone signal, responsive to a sound pressure on the microphone element, to the input ($\phi$) of the microphone preamplifier.

20. (original) A microphone comprising an integrated circuit as set forth in any of the above claims and a MEMS microphone element to provide a microphone signal, responsive to a sound pressure on the MEMS microphone element, to the microphone preamplifier.